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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/756,763	01/14/2004	Masahiro Sunohara	040001	1523
23850	7590	12/16/2005	EXAMINER	
ARMSTRONG, KRATZ, QUINTOS, HANSON & BROOKS, LLP			WILLIAMS, ALEXANDER O	
1725 K STREET, NW			ART UNIT	PAPER NUMBER
SUITE 1000				
WASHINGTON, DC 20006			2826	

DATE MAILED: 12/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/756,763	SUNOHARA ET AL.
Examiner	Alexander O. Williams	Art Unit 2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

Disposition of Claims

4) Claim(s) 1-17 is/are pending in the application.
4a) Of the above claim(s) 1-12 and 14 is/are withdrawn from consideration.
5) Claim(s) _____ is/are allowed.
6) Claim(s) 13 and 15 to 17 is/are rejected.
7) Claim(s) _____ is/are objected to.
8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 7/16/6/16&1/14/05.
4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ .
5) Notice of Informal Patent Application (PTO-152)
6) Other: ____ .

Serial Number: 10/756763 Attorney's Docket #: 040001
Filing Date: 1/14/2004; foreign priority to 1/23/03 and 11/17/03

Applicant: Sunohara et al.

Examiner: Alexander Williams

Applicant's election of species I, figures 2A-2H (claims 13 and 15 to 17), filed 10/25/05 to the election of Group I, claims 13-17 filed 7/29/05 has been acknowledged.

This application contains claims 1 to 12 and 14 drawn to an invention non-elected with traverse.

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:
A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 13 and 15 to 17 are rejected under 35 U.S.C. § 102(b) as being anticipated by Gorczyca (U.S. Patent # 5,492,586).

13. Gorczyca (figures 1 to 11) specifically figure 12 show an electronic parts packaging structure comprising: a wiring substrate **14,10,16** including a wiring pattern **36**; a first insulation film **18** formed on the wiring substrate; an electronic parts **20** having a connection terminal **22** on an element formation surface (**top of 20 and bottom of 26**), the electronic parts being buried in the first insulation film in a state where the connection terminal is directed upward and being mounted in a state where a backside of the electronic parts is not in contact with the wiring substrate; a second insulation film **26,28** for covering the electronic parts; via holes **30,34** respectively formed in a predetermined portion of the first and second insulation films on the wiring pattern and

the connection terminal; and an upper wiring pattern 32 formed on the second insulation film, the upper wiring pattern being connected to the wiring pattern and the connection terminal through the via holes.

15. The electronic parts packaging structure according to any one of claims 13 and 14, Gorczyca show wherein the element formation surface of the electronic parts and an upper surface of the insulation film in which the electronic parts is buried are at an almost same height to be planarized.

16. The electronic parts packaging structure according to any one of claims 13 and 14, wherein the electronic parts is a semiconductor chip having a thickness of approximately 150 micrometer or less.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

17. The electronic parts packaging structure according to any one of claims 13 and 14, Gorczyca show wherein the insulation film is made of resin.

Initially, it is noted that the 35 U.S.C. § 103 rejection based on a first insulating film and a second insulating film deals with an issue (i.e., the integration of multiple pieces into one piece or conversely, using multiple pieces in replacing a single piece) that has been previously decided by the courts.

In Howard v. Detroit Stove Works 150 U.S. 164 (1893), the Court held, "it involves no invention to cast in one piece an article which has formerly been cast in two pieces and put together...."

In In re Larson 144 USPQ 347 (CCPA 1965), the term "integral" did not define over a multi-piece structure secured as a single unit. More importantly, the court went further and stated, "we are inclined to agree with the solicitor that the use of a one-piece construction instead of the [multi-piece] structure disclosed in Tuttle et al. would be merely a matter of

obvious engineering choice" (bracketed material added). The court cited In re Fridolph for support.

In re Fridolph 135 USPQ 319 (CCPA 1962) deals with submitted affidavits relating to this issue. The underlying issue in In re Fridolph was related to the end result of making a multi-piece structure into a one-piece structure. Generally, favorable patentable weight was accorded if the one-piece structure yielded results not expected from the modification of the two-piece structure into a single piece structure.

Claims 13 and 15 to 17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Eichelberger (U.S. Patent # 5,111,278).

13. Eichelberger (figures 1 to 18) specifically figure 2 show an electronic parts packaging structure **20** comprising: a wiring substrate **30** including a wiring pattern **32,24,34**; a first insulation film (**33, half of 42 up until it reaches the surface level of 38**) formed on the wiring substrate; an electronic parts **38** having a connection terminal (**on 38 and connected to 44**) on an element formation surface (**level of 42 where the top of 38 in parallel**), the electronic parts being buried in the first insulation film (**lower portion of 42**) in a state where the connection terminal is directed upward and being mounted in a state where a backside of the electronic parts is not in contact with the wiring substrate; a second insulation film (**portion of 42 above 38 and 36**) for covering the electronic parts; via holes (**vias in which 44,46 lie within**) respectively formed in a predetermined portion of the first and second insulation films on the wiring pattern and the connection terminal; and an upper wiring pattern **44,46** formed on the second insulation film, the upper wiring pattern being connected to the wiring pattern and the connection terminal through the via holes.

15. The electronic parts packaging structure according to any one of claims 13 and 14, Eichelberger et al. show wherein the element formation surface (**level of 42 where the top of 38 exist**) of the electronic parts and an upper surface of the insulation film in which the electronic parts is buried are at an almost same height to be planarized.

16. The electronic parts packaging structure according to any one of claims 13 and 14, Eichelberger et al. show wherein the electronic parts is a semiconductor chip having a thickness of approximately 150 micrometers or less.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

17. The electronic parts packaging structure according to any one of claims 13 and 14, Eichelberger et al. show wherein the insulation film is made of resin.

Therefore, it would have been obvious to one of ordinary skill in the art to use the first insulating film and the second insulating film as "merely a matter of obvious engineering choice" as set forth in the above case law.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/774,773,758,211,203,207,208,730	12/9/05
Other Documentation: foreign patents and literature in 257/774,773,758,211,203,207,208,730	12/9/05
Electronic data base(s): U.S. Patents EAST	12/9/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
12/9/05